REMARKS

Claims 1-46 stand rejected. Claims 1, 8, 20, 34, 37 and 44 have been amended to set forth the recited subject matter more clearly. Reconsideration of the application in view of the remarks set forth below is respectfully requested.

Rejections under 35 U.S.C. § 112

The Examiner rejected claims 40 and 44 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. With regard to claim 40, the Examiner stated, "it is unclear whether the phrase 'store a request corresponding to a request' should read 'store an index corresponding to a request' to match other presented independent claims. Correction or clarification is therefore required."

Applicant respectfully submits that the claim currently recites the intended subject matter. Specifically, claim 40 is directed to a queue structure comprising an entry shifter, rather than an index shifter, as recited in the other independent claims. As described on page 32, lines 7-17 of the present specification, in an alternate configuration, instead of storing and shifting the index for a particular request to allow for out-of-order processing, the queue entries (i.e., the requests) themselves may be stored in an entry shifter comprising a plurality of shift registers. Accordingly, claim 40 recites an entry shifter configured to store a request. Applicant respectfully submits that claim 40 is not indefinite and respectfully requests withdrawal of the Examiner's rejection.

With specific regard to claim 44, the phrase "the entry read flag" has been amended to recite "the entry ready flag." Applicant respectfully submits that claim 44 is in compliance

with 35 U.S.C. § 112, second paragraph, and respectfully requests withdrawal of the Examiner's rejection.

Rejections under 35 U.S.C. § 103

The Examiner rejected claims 1-4, 7-14, 18-26, 30-43 and 46 under 35 U.S.C. § 103(a) as being unpatentable over Chin et al (U.S. 6,356,972). Further, the Examiner rejected claims 17 and 29 under 35 U.S.C. § 103(a) as being unpatentable over Chin et al (U.S. Pat. No. 6,356,972), in view of Schrofer (U.S. Pat. No. 4,682,284). With specific regard to the independent claims, the Examiner stated:

> As to claim 40, Chin et al teach a queue entry pool comprising a plurality of fixed registers configured to store requests (figure 4, queues 66 or 68), and an entry shifter coupled to the queue entry pool (figure 4, In-Order queue 64) and comprising a plurality of registers, each of the registers is configured to store a request corresponding to a request stored in one of the plurality of fixed registers (col. 5 lines 35-65 and col. 11 line 9 – col. 12 line 67).
>
> However, Chin et al do not expressly teach the entry shifter registers being shift registers. It would have been obvious for one of ordinary skill in the art at the time of the invention to modify teachings of Chin et al to utilize such well known shift registers so that the system may perform entry shifting in an efficient manner.
>
> As to claim 1, Chin et al teach all of the limitations as stated above in claim 40. In addition, Chin et al teach each entry shifter register corresponds to one of the plurality of fixed registers (col. 11 lines 9-62).
>
> As to claim 8, Chin et al teach all of the limitations as stated above in claims 40 and 1. In addition, Chin et al teach a plurality of processor controller interfaces configured to receive requests from one of a processor bus and an I/O bus, each request having a corresponding request type, and a plurality of queues coupled to each of the processor controller interfaces and configured to store requests, wherein each request is delivered to one of the plurality of queues depending on the origin of the request and the request type (figure 4, lines 9-24).

> As to claim 20, Chin et al teach all of the limitations as stated above in claims 1 and 8. In addition, Chin et al teach one or more processors and a memory controller coupled to the one or more processors (col. 7 lines 23-34).
>
> Claims 34-39 are directed to the method of system claims 1-4, 7-14, 18-26, 30-43 and 46. Chin et al teach the system as set forth in claims 1-4, 7-14, 18-26, 30-43, and 46. Therefore, Chin et al also teach the method as set forth in claims 34-39.

The burden of establishing a *prima facie* case of obviousness falls on the Examiner. *Ex parte Wolters and Kuypers*, 214 U.S.P.Q. 735 (PTO Bd. App. 1979). Obviousness cannot be established by combining or modifying the teachings of the prior art to produce the claimed invention absent some teaching or suggestion supporting the combination or modification. *See ACS Hospital Systems, Inc. v. Montefiore Hospital*, 732 F.2d 1572, 1577, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984). Accordingly, to establish a *prima facie* case, the Examiner must not only show that the combination includes *all* of the claimed elements, but also a convincing line of reason as to why one of ordinary skill in the art would have found the claimed invention to have been obvious in light of the teachings of the references. *Ex parte Clapp*, 227 U.S.P.Q. 972 (B.P.A.I. 1985). For a single prior art reference, the mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification. *See In re Fritch*, 23 U.S.P.Q.2d 1780, 1783-84 (Fed. Cir. 1992).

Applicant respectfully traverses the Examiner's rejections for at least three reasons. First, as admitted by the Examiner, the Chin reference does not disclose an index shifter or an entry shifter comprising a plurality of shift registers. However, contrary to the Examiner's assertion, Applicant respectfully submits that it would not have been obvious for one of ordinary skill in the art to modify the teachings of Chin to utilize shift registers as recited in

independent claims 1, 8, 20, 34, 37 and 40. Second, the Chin reference does not even disclose an index shifter, much less an index shifter configured to store *only* an index, as recited in claims 1, 8, 20, 34 and 37, as amended. Third, the Chin reference does not disclose a queue entry pool comprising a plurality of fixed registers configured to store a plurality of flags corresponding to the *status* of each request, as recited in dependent claims 3, 13, 25 and 42, much less a plurality of flags comprises each of a valid entry flag, an entry ready flag and a retire flag, as recited in dependent claims 4, 14, 26 and 43.

Independent claims 1, 8, and 20 each recite "an index shifter...comprising a plurality of shift registers." Similarly, independent claims 34 and 37 recite acts associated with a shift register. Generally speaking, the index shifter includes a plurality of registers, each corresponding to an entry slot in the queue entry pool (page 26, lines 21-22). As a request is stored in the queue entry pool, the index referencing that request in injected into the "head" end of the index shifter. Page 26, lines 21-23. As new indices are injected into the head of the index shifter due to the new requests being stored in the new queue pool, the indices are pushed to the next register in the index shifter. Page 26, line 23 – page 27, line 1. Thus, the oldest index (corresponding to the oldest request in the queue entry pool) is always closer to the "tail" of the index shifter than any new indices. Page 27, lines 1-3. The shifting operation guarantees that if an entry anywhere in the index shifter points to an invalid register in the queue entry pool, then each shift register in the index shifter between the available one and the head moves immediately toward the tail. Page 27, lines 16-18. Because the requests in the queue entry pool remain in the slot in which they were placed until the request is retired, it is the corresponding index that is stored in the index shifter in a particular shift register that shifts and dictates the order of request processing. Page 30, lines 14-16. The index stored in

the index shifter retains information corresponding to the particular slot in which a request is stored in the queue entry pool. Page 30, lines 16-18.

Similarly, claim 40 recites "an entry shifter....comprising a plurality of shift registers." As previously discussed, claim 40 is directed to a queue structure comprising an entry shifter, rather than an index shifter. As described on page 32, lines 7-17 of the present specification, in accordance with this exemplary embodiment, instead of storing and shifting the index for a particular request to allow for out-of-order processing, the queue entries (i.e., the requests) themselves may be stored in an entry shifter comprising a plurality of shift registers.

The Examiner correlated the peripheral request queue 66 and the memory request queue 68 disclosed in the Chin reference with the recited queue entry pool. The Examiner further correlated the in-order queue 64 with the recited index shifter and the recited entry shifter. With regard to the first point, as admitted by the Examiner, the Chin reference does not disclose shift registers. However, contrary to the Examiner's assertion, Applicant respectfully submits that it would not have been obvious to modify the Chin reference such that the in-order queue 64 comprised a plurality of shift registers, since there is absolutely no suggestion in the Chin reference to make such a modification. Indeed, the Chin reference discloses mechanisms for maintaining the order of data sent to and from memory and I/O space, *without* implementing a shift register to track the entries. One skilled in the art would not be motivated to modify the in-order queue 64 to provide a shift register for maintaining request processing order, since Chin already discloses other techniques for doing such.

As admitted by the Examiner, the Chin reference does not disclose an index shifter or an entry shifter comprising a plurality of shift registers. For the reasons set forth above, Applicant submits that one skilled in the art would not be motivated to modify the in-order queue 64 in the manner recited in each of the independent claims, and thus, the Chin reference cannot possibly render the recited subject matter obvious. Accordingly, for this reason alone, Applicant respectfully submits that independent claims 1, 8, 20, 34, 37 and 40 are allowable.

With regard to the second point, claims 1, 8, 20, 34 and 37 an index shifter configured to store *only* an index. As explicitly stated in the Chin reference, the in-order queue 64 is configured to store the entry number, request type and snoop results. Col. 11, lines 39-41. By storing this additional information, the in-order queue may be disadvantageously large.

In contrast, since the shift registers in the index shifter only retain location information, (i.e., the index) the registers need only be configured to provide enough storage for one corresponding index. Page 30, lines 20-22. For instance, if the queue entry pool only comprises 4 fixed registers, each shift register only needs to include enough storage space for two bits to store each binary index 00,01,10 and 11. Page 30, line 22 – page 31, line 1. Similarly, for a queue entry pool with 16 fixed registers, 16 four bit shift registers may be implemented. Page 31, lines 1-2. By using the index shifter and comprising a plurality of shift registers, the configuration described in the present specification and recited in the present claims, permits out-of-order retirement of requests in the system. Page 31, lines 16-17.

Because the Chin reference does not disclose an index shifter configured to store *only* an index corresponding to a request stored in the queue entry pool, as recited in independent claims 1, 8, 20, 34 and 37, Applicant submits that the Chin reference cannot possibly render the recited subject matter obvious. Accordingly, for this additional reason, Applicant respectfully submits that independent claims 1, 8, 20, 34 and 37 are allowable.

With regard to the third point, dependent claims 3, 13, 25 and 42 recite a queue entry pool comprising a plurality of fixed registers configured to store a plurality of flags corresponding to the status of each request. Applicant respectfully submits that the Chin reference does not disclose storing a plurality of flags corresponding to the status of the request in the queues. As explicitly stated in the Chin reference, the only information stored in the queues 66 and 68 is the address, entry number and request type of the corresponding request. In stark contrast, claims 3, 13, 25 and 42 recite storing a plurality of flags corresponding to the *status* of each request. As described in the present specification, a variety of information corresponding to a request may be stored in a respective field in the queue entry pool. Page 22, lines 4-5. Fields such as a valid entry field, entry ready field, entry sent field or entire entry field may be stored in the queue entry field for each request, for instance. Page 22, lines 5-7. Exemplary field descriptions are provided on pages 22 and 23 of the present specification, for instance.

Generally, the fields stored for each request in the queue entry pool, may create a state machine providing a roadmap for the processing of the requests in the queue entry pool. Page 23, lines 15-16; *see* e.g., Fig. 6. The specific fields and the sequence of execution dictated by these fields may be specific and unique for a particular system design. Page 23, lines16-17. It is sufficient to know that various information delivered with each request and with

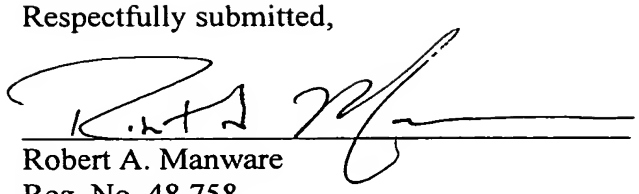
corresponding control signals are stored in the queue entry pool such that they may be interpreted and used by other components of the sub-system to prioritize the processing of the requests in the queue entry pool. Page 23, lines 18-21. The Chin reference simply does not disclose or suggest storing this type of information in a queue along with a request. In fact, as described above, the Chin reference explicitly states that the queues 66 and 68 only store address, entry number and request type. Accordingly, the Chin reference cannot possibly disclose fixed registers configured to store a plurality of flags corresponding to the status of a request as recited in claims 3, 13, 25 and 42, much less disclose that the flags comprise a valid entry flag, an entry ready flag and a retire entry flag as further recited in claims 4, 14, 26 and 43. For this additional reason, Applicant respectfully submits that the Chin reference cannot possible render the recited subject matter obvious.

For at least the reasons set forth above, Applicant respectfully submits that the Chin reference fails to disclose all of the recited features or suggest a basis for modifying the teaching of Chin in the matter recited in the present claims. Applicant further notes that the Schrofer reference fails to cure the deficiencies of the Chin reference. Accordingly, Applicant respectfully requests withdrawal of the Examiner's rejections under 35 U.S.C. § 103 and allowance of claims 1-46.

Conclusion

In view of the remarks set forth above, Applicants respectfully request reconsideration of the Examiner's rejections and allowance of claims 1-46. If the Examiner believes that a telephonic interview will help speed this application toward issuance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,



Date: June 24, 2004

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